AMENDMENT TO THE SPECIFICATION

Please replace the first paragraph on page 1 of the English translation with the following heading, subheading and marked-up paragraph:

--Background of the invention

Field of the Invention

The invention relates to a method of manufacturing filled isolation trenches in silicon by applying Complementary Metal Oxide Semiconductor (CMOS) standard processes for forming dielectrically insulated regions (insulation trenches; isolation trenches) on [[an]] a Silicon on Insulator (SOI) wafer. To this end, only silicon dioxide (SiO_2) is to be used for the filling. The technique results in sealed cavities of voids within the trench. These remaining voids are advantageous with respect to a reduction of elastic stress. The technique leads to the filling of trenches having an aspect ratio ranging from small values to very high values with various angles of the sidewalls.--

Please insert the following subheading before the second full paragraph beginning "The conventional isolation trenches for the dielectric . . ." on page 1 of the English translation:
--Description of related art--

Please insert the following heading before the third full paragraph beginning "It is an object of the present invention to provide a cost effective realization of . . ." on page 2 of the English translation:

--Brief summary of the invention--

Please insert the following heading before the sixth full paragraph beginning "The invention will be described and completed by embodiments including two . . ." on page 2 of the English translation:

--Brief description of the several views of the drawings--

Please insert the following heading before the fourth paragraph beginning "Figures 1 and 1b illustrate the trench 2 etched into the silicon 1 as an example of an . . ." on page 3 of the English translation:

--Detailed description of the invention--

Please replace the sixth full paragraph on page 4 of the English translation with the following marked-up paragraph:

--SiO_2 is again deposited, preferably by [[an]] a low pressure technique and a sealing layer 10 is formed within and on the at least one trench 2, as illustrated in figures 4a and 4b. The layer 10 extends across the remaining layers 7a, the steps at both sides and onto the horizontal surfaces outside the trench 2.--

Please replace the second full paragraph on page 5 of the English translation with the following marked-up paragraph:

--The filling in the first fill step is adapted to or controlled with respect to "the trench geometry". The silicon dioxide deposition 7 providing the horizontal sections at both sides of the trench 2 and the vertical sections 7', 7" inside the trench 2 is adapted to the trench geometry, which has the upper corner areas and substantially vertical walls in the depth direction of the trench 2 as well as a substantially horizontal surface of the active semiconductor layer 1. Due to the trench geometry, the thickened portion of the deposited inner layer (inside the trench 2) is formed during the first deposition, wherein the left layer and the right layer in the vicinity of the trench edges 2a', 2a" (in the height area) grow more strongly or intensively, thereby increasingly forming a bottleneck 8, which has, as a bottleneck, a reduced width compared to the free volume 9 in the form of "remaining trench or residual trench", the width of which increases with increasing depth.--

Please replace the third full paragraph on page 5 of the English translation with the following marked-up paragraph:

--Since the bottleneck 8 is substantially independent of the trench depth, that is, the aspect ratio, and is substantially independent of the angle of the trench walls near the silicon surface, the position of a sealing point to be formed in a later stage is realized independently of the trench geometry. The controlled silicon dioxide deposition adapted to the trench geometry is meant as a deposition that is adapted to the ~~illustrates~~ illustrated trench geometry; the bottleneck 8 is automatically obtained, even and in particular with substantially vertical trench walls 1a', 1a". In this case the effect is taken advantage of that the silicon dioxide is deposited faster (at interfaces of faces parallel to the surface and faces having a vertical part, in the present case, the entire side faces facing inwardly or the inner surfaces of the trenches). The tapering of the entrance of the remaining void 9, that is, the largest bottleneck 8 of the trench 2, is obtained near the edges and is not avoided but instead is advantageously exploited.--

Please replace the first full paragraph on page 6 of the English translation with the following marked-up paragraph:

--The SOI wafer may be structured such that in its semiconductor layer located above the oxide layer, ~~also~~ micro mechanic systems (MEMS) are also provided, which are not explicitly shown.--

Please replace the second full paragraph on page 6 of the English translation with the following marked-up paragraph:

--The second step of removing the SiO_2 layer, explained with reference to figures 3a and 3b, shall be emphasized once again in order to explain the sealing or closing point 12, which is located in the respective embodiments below the respective surfaces 3b, 4b according to the respective figures 4a and 4b.--

Please replace the third full paragraph on page 6 of the English translation with the following marked-up paragraph:

--The exemplary anisotropic reactive ion etching (RIE) etch process of the oxide layer 7 in figures 2a and 2b results in two symbolical sub steps, thereby firstly removing the horizontal layer portions, as is shown in figures 3a and 3b. This is the "first sub step" that is performed until the removal of the silicon dioxide layer on the wafer surface.--

Please replace the fourth full paragraph on page 6 of the English translation with the following marked-up paragraph:

--From then on the symbolic "second sub step" follows. Hereby, a portion of the silicon dioxide layer 7a provided at the vertical trench walls 1a', 1a" is also removed and the bottleneck 8 is displaced downwardly. In the upper trench portion, the oxide layer is thus removed down to a defined depth, as is shown as a7 in figure 3a and a8 in figure 3b. Due to this material removal and the displacement of the bottleneck in the depth direction the later sealing point is determined, which is then actually formed by the further deposition of silicon dioxide of figures 4a and 4b. The sealing point is located at the downwardly displaced bottleneck 8a, from which is obtained the upper sealing point 12, that is, the upper end of the sealed void 11, after the further deposition. This is simultaneously the lower end of the portion 14 of the hermetic sealing.--

Please insert the heading and paragraph on the following page as an Abstract of the Disclosure as a separate page numbered page 11: